In the Claims

The claims in this application are being submitted in accordance with the revised format detailed in the *Official Gazette* on February 25, 2003.

1. (Original) An apparatus comprising:

a processor;

an operating system to control a plurality of power management states, one of said power management states being a low latency low power state;

a memory subsystem that requires initialization commands to exit a memory low power state;

control logic to detect exiting of said low latency low power state and to responsively generate a plurality of initialization commands to remove said memory subsystem from said memory low power state prior to allowing execution of the processor to resume.

2. (Original) The apparatus of claim 1 wherein said low latency low power state is a state from which the apparatus resumes without executing BIOS routines.

3. (Original) The apparatus of claim 1 wherein the low latency low power state is an ACPI S1 state and wherein said memory low power state is one of a nap state and a powerdown state.

4. (Original) The apparatus of claim 1 wherein said control logic comprises:

low power state exit detection logic;

memory resume sequencing logic.

B1

5. (Original) The apparatus of claim 4 wherein said memory resume sequencing logic is to receive an indication of exiting the low latency low power state from the low power state exit detection logic and is to allow deassertion of a stop clock signal after said plurality of initialization commands have been executed by the memory resume sequencing logic.

Sub C1

6. (Original) The apparatus of claim 5 wherein said memory resume sequencing logic is included in a memory interface and said low power state exit detection logic is included in an I/O control hub (ICH), said apparatus further comprising:

first messaging logic to transmit a low power state exit message to said memory interface;

second messaging logic to transmit an end of low power state exit message back to said ICH after said memory interface completes said plurality of initialization commands in response to said low power state exit message.

7. (Original) The apparatus of claim 1 wherein said plurality of initialization commands comprises:

initializing memory interface control logic;

waiting for a clock circuit to lock;

setting a current control register;

performing memory core initialization operations.

8. (Original) The apparatus of claim 7 wherein setting the current control register comprises setting the current control register to a midpoint value.

B1

9. (Original) The apparatus of claim 7 wherein performing memory core initialization operations comprises performing a sequence of pre-charge and refresh operations.

Sub C1

10. (Original) An apparatus comprising:

messaging logic coupled to receive a low power state exit message;

memory system resume logic coupled to receive said low power state exit message from said messaging logic, said memory system resume logic to sequence through a plurality of initialization commands prior to generating a signal to cause a processor to exit a low power state.

11. (Original) The apparatus of claim 10 wherein said messaging logic is further to return an end of low power state exit message subsequent to completion of said plurality of initialization commands by said memory system resume logic.

12. (Original) The apparatus of claim 11 further comprising:

low power state exit detection logic to detect an exiting condition for one of a plurality of a low power states and to generate the low power state exit

message.

13. (Original) The apparatus of claim 12 wherein the signal is a deassertion of a stop clock signal which is generated in response to said end of low power state exit message.

B1
Sub C1

14. (Original) The apparatus of claim 13 wherein said low power state is an ACPI S1 state.

15. (Original) The apparatus of claim 10 wherein said plurality of initialization commands comprise:

initializing memory interface control logic;

waiting for a clock circuit to lock;

setting a current control register;

performing memory core initialization operations.

16. (Original) The apparatus of claim 15 wherein setting the current control register comprises setting the current control register to a midpoint value.

17. (Original) The apparatus of claim 15 wherein performing memory core initialization operations comprises performing a sequence of pre-charge and refresh operations.

18. (Previously Amended) A method comprising:

detecting an event to cause an exit from a low latency low power state;

initializing a memory subsystem transparently to execution resources of a processor that is starting operations in response to the exit from the low latency low power state;

exiting the low latency low power state.

B1

Sub C1

19. (Original) The method of claim 18 wherein initializing comprises:

initializing memory interface control logic;

waiting for a clock circuit to lock;

setting a current control register;

performing memory core initialization operations.

20. (Original) The method of claim 19 wherein setting the current control register comprises setting the current control register to a midpoint value.

21. (Original) The method of claim 19 wherein performing memory core initialization operations comprises performing a sequence of pre-charge and refresh operations.

22. (Original) The method of claim 18 wherein detecting comprises:

reading a bit set by BIOS upon entry into said low latency low power state;

sending a resume message from an I/O control hub to memory interface logic.

23. (Previously Amended) The method of claim 22, after initializing, further comprising:

returning an initialization complete message to the I/O control hub;

deasserting a stop clock signal.

B1 end

24. (Original) The method of claim 18 wherein exiting the low latency low power state comprises deasserting a stop clock signal to a processor.

Sub C1

25. (Original) The method of claim 18 further comprising:

detecting a low power state entry condition;

setting a bit to indicate to indicate the low latency low power state is selected from a plurality of low power states.

---

26. (New) A system comprising:

B2

a processor;

a memory;

Sub C1

an input/output controller to generate a first low power message to signal an exit of a low power state and to send a second low power message to the processor;

a memory controller coupling the processor to the memory, the memory controller to receive the first low power message and to responsively generate a plurality of initialization commands for the memory and to generate a first responsive message to the input/output controller, the second low power message being sent to the processor by the input/output controller responsively to the first responsive message sent to the input/output controller from the memory

controller.

27. (New) The system of claim 26 wherein the processor and the memory controller are portions of an integrated processor device including both the processor and the memory controller.

28. (New) The system of claim 26 wherein said low power state is a state from which the processor resumes without executing BIOS routines.

29. (New) The system of claim 26 wherein said plurality of initialization commands comprises:

waiting for a clock circuit to lock;

setting a current control register to a midpoint value.

30. (New) The system of claim 26 further comprising a BIOS routine to set a bit upon entry into the low power state.

31. (New) The system of claim 30 wherein the bit is a bit written to in the memory controller.

32. (New) The system of claim 31 wherein said low power state is a state from which the processor resumes without executing BIOS routines.